



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

NIGHTINGALE

Atty. Ref.: 550-286

Serial No. 09/994,023

Group: 2128

Filed: November 27, 2001

Examiner: Alhija, Saif A.

For: HARDWARE SIMULATION USING A TEST SCENARIO
MANAGER

Before the Board of Patent Appeals and Interferences

REPLY BRIEF FOR APPELLANT

**On Appeal From Final Rejection
From Group Art Unit 2128**

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January 25, 2008

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY BRIEF

Sir:

This is a reply to the Examiner's Answer dated November 26, 2007.

Nothing in the Answer overcomes the basic deficiencies in Rajsuman pointed out in the Brief. One deficiency is that Rajsuman lacks the claimed shared memory used by a signal interface controller to store data that is readable from that same memory by another signal interface controller. On page 4 of the Examiner's Answer, the Examiner contends that this claim element is disclosed in column 7, line 60 to column 8, line 5 and Figure 5 of Rajsuman. That text is quoted here in its entirety:

As shown in Fig. 5, each pin-group (assigned verification unit) also contains a control CPU 67 that controls the data flow, application of simulation data to the silicon ICs 68₁-68₅, response comparison, scheduling of various tasks for individual blocks/cores as well as monitoring the status of individual cores (silicon ICs) and SoC. The control CPUs

67₁-67₆ are connected with one another. The control CPUs 67₁-67₆ are also connected to the main system CPU through the bus system 64. In the design validation station DVS₆ for glue logic, a synchronization unit 75 and an arbitration unit 76 are provided to promote data transfer to and from the main system CPU 62 and the control CPUs 67₁-67₆ of design validation stations DVS₁-DVS₆.

Nothing in this text describes a shared memory included within the test scenario manager which may store data from one signal interface controller (which Examiner equates with a verification unit (VU) 66 of Rajsuman) which is readable from the shared memory by another signal interface controller (another VU). Nor does Figure 5 show the claimed shared memory.

On page 7 of the Answer, the Examiner states that column 13, lines 5-15 shows that the CPU deals with tasks such as synchronization when evaluating the overall SoC. The Examiner then contends that “since the VUs are connected to each other as well they therefore possess [sic] a shared memory.” (Emphasis added). This statement is incorrect and illogical. The claims recite: “wherein said test scenario manager includes a shared memory into which a signal interface controller may store data....” Thus, it is the test scenario manager that includes the shared memory, not the VUs. The Examiner’s statement that “they” (i.e., the VUs) possess a shared memory is therefore both irrelevant and incorrect. The fact that the VUs are connected does not have any bearing on whether the test scenario manager (which the Examiner maps to the system CPU 62 of Rajsuman) has the claimed shared memory. Nor is a connection the same as a shared memory.

The Examiner states on page 8 that “[s]ince the Main CPU carries out synchronization, response evaluation of cores, timing evaluation, and overall SoC

evaluation etc. the Main CPU possesses the shared data memory to allow for complete evaluation of the SoC.” Where in this text does Rajsuman teach that a shared memory is used to store data from a signal interface controller (mapped to a VU in Rajsuman) that is then readable from that shared memory by another signal interface controller, i.e., another VU in Rajsuman? That Rajsuman’s CPU performs a complete evaluation of the SoC does not disclose that data supplied by one VU is accessible by any of the other VUs. Indeed, the Examiner fails to point out where Rajsuman explains that one VU would even have a need to read information supplied by another VU.

The Examiner also argues that “[t]his is further reinforced in Figure 5 for example where the overall SoC evaluation must evaluate a memory [*note – this memory is one of the silicon cores being validated and cannot be the claimed shared memory*], function, bus, processor etc. in conjunction, therefore the arbitration, synchronization, and overall evaluation utilizes multiple VUs connected together via the CPU and provided data to each other via the CPU.” (The bracketed note and underlined emphasis are added). Nothing in Figure 5 shows that the VUs provide data to each other via the CPU 62. Again, just because the CPU uses data from multiple VUs in its overall evaluation does not mean that those VUs provide data to each other.

Rajsuman also does not disclose storing data independent of advancement of simulated time as claimed. The Examiner cites column 12, lines 15-52 of Rajsuman which describes how the CPU performs a “Fork” operation on an application task to “break it into multiple sub-tasks, schedule them and assign these sub-tasks to different VUs that are mapped to individual cores... Thus, the system compiler with multiple

distribution control can perform “Fork” on the application task to execute it in a distributed computing environment made up of the multiple verification units.” Thus, different parts of the SoC (i.e., different IC’s or cores) in Rajsuman may be executed at different times. But the Examiner then erroneously concludes on page 11 that “[t]his section indicates that different parts of the SoC are executed at different times, which requires time defining events that either advance or slow down the execution of an event.” (Emphasis added). The Examiner’s underlined conclusion does not follow logically from the premise. Just because different parts of the SoC are executed at different times does not mean that execution of an event must be advanced or slowed down. Nor does the Examiner supply any evidence in Rajsuman of advancing or slowing down execution of an event. The underlined text from the quote of column 12, line 19 above simply states that the multiple sub-tasks are scheduled by the CPU. The CPU just arranges at what time the event begins. Scheduling does not require the execution of the sub-task to be advanced or slowed down. Nothing in Rajsuman states that time itself is advanced or slowed down or that data is stored independently of the advancement of simulated time.

The Examiner also argues that the synchronization clock unit 75 in Rajsuman performs this claim feature. It is now more apparent that the Examiner is mapping to the synchronization clock unit 75 to the claimed time generator, which is another error in the rejection. The claimed time generator “generat[es] messages specifying time defining events corresponding to advancement of simulated time for said hardware simulator.”

The synchronizing clock unit 75 synchronizes the VUs—not the silicon ICs. See column

8, lines 2-4, which states that the synchronizing clock unit 75 is “provided to promote data transfer to and from the main system CPU 62 and the control CPUs 67₁-67₆,” and column 12, lines 29-33: the clock unit 75 allows “the communication and error-free data transfer from the main system CPU 62 to control CPUs 67 of the individual VUs 66.” Thus, the synchronization clock unit 75 regulates transfer between the main system CPU 62 and the control CPUs 67 of the individual VUs 66.

So the synchronization clock unit 75 only acts on the main system CPU and the VUs, but not on the silicon ICs which the Examiner maps to the claimed hardware simulator. Thus, the synchronization clock unit 75 is not the claimed time generator. Indeed, nothing in Rajsuman describes changing the simulated time of the silicon ICs. Nor can the Examiner point out where Rajsuman describes the synchronizing clock unit 75 being used to store data independently of the advancement of simulated time.

The Examiner states on page 11 that: “Appellants seem to argue that the references’ buses will take longer to enable communication than the shared data memory disclosed in the claims however the Examiner is puzzled by this assertion since as per paragraphs 35 and 39 of the specification of the instant application, Appellants claimed XVCs (External Verification Controllers) are also connected via a bus.” The Examiner confuses the difference between “real time” and “simulated time.” Real time is the actual time which it takes for information to be communicated over a bus. Simulated time is defined by the control clock of the hardware simulation. If the control clock does not change, then no simulated time passes for the hardware simulation (although real time still passes). Even though a bus used in conjunction with the apparatus in claim 1 and the

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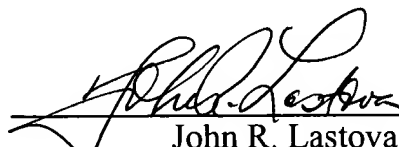
bus of Rajsuman may take the same amount of real time to communicate information, the bus used in conjunction with the apparatus in claim 1 takes a shorter amount of simulated time. This is because, unlike in Rajsuman, the claimed time generator controls the advancement of simulated time for the hardware simulation. Rajsuman's synchronization unit 75 does not do this. The claimed time generator allows information to be passed backwards and forwards on the bus while the simulated time of the hardware simulation is stopped. This is not possible in Rajsuman. As a result, the control clock of the hardware simulation continues to run while information is being sent, which means that Rajsuman takes more simulated time to transfer information.

Rajsuman lacks multiple features recited in the independent claims including the claimed time generator, shared memory writeable and readable by the signal interface controllers, and storing of data in shared memory "independently of advancement of simulated time by said messages specifying time defining events." The Board should reverse the final rejection.

Respectfully submitted,

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